CM1231-02SO

2, 4 and 8-Channel Low-Capacitance ESD Protection Array

The CM1231−02SO is a member of the XtremeESD™ product family and is specifically designed for next generation deep submicron ASIC protection. These devices are ideal for protecting systems with high data and clock rates and for circuits requiring low capacitive loading such as USB 2.0.

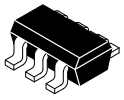
The CM1231−02SO incorporates the PicoGuard XP™ dual stage ESD architecture which offers dramatically higher system level ESD protection compared with traditional single clamp designs. In addition, the CM1231−02SO provides a controlled filter roll−off for even greater spurious EMI suppression and signal integrity.

The CM1231−02SO protects against ESD pulses up to ±12 kV contact on the “OUT” pins per the IEC 61000−4−2 standard.

The device also features easily routed “pass−through” differential pinouts in a 6−lead SOT23 package.

- Two Channels of ESD Protection
- Exceeds ESD Protection to IEC61000−4−2 Level 4:
  - ±12 kV Contact Discharge (OUT Pins)
- Two−Stage Matched Clamp Architecture
- Matching−of−Series Resistor (R) of ±10 mΩ Typical
- Flow−Through Routing for High−Speed Signal Integrity
- Differential Channel Input Capacitance Matching of 0.02 pF Typical
- Improved Powered ASIC Latchup Protection
- Dramatic Improvement in ESD Protection vs. Best in Class Single−Stage Diode Arrays
  - 40% Reduction in Peak Clamping Voltage
  - 40% Reduction in Peak Residual Current
- Withstands over 1000 ESD Strikes*
- Available in a SOT23−6 Package
- These Devices are Pb−Free and are RoHS Compliant

- USB Devices Data Port Protection
- General High−Speed Data Line ESD Protection



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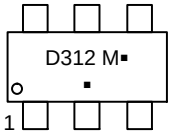


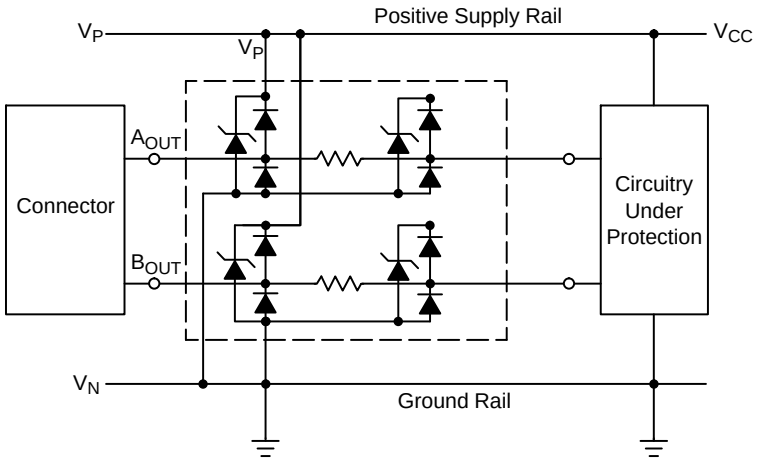
D312 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

		†
CM1231−02SO	SOT23−6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*Standard test condition is IEC61000−4−2 level 4 test circuit with each (A_{OUT}/B_{OUT}) pin subjected to ±12 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run.

Publication Order Number:


Positive Supply Rail
V_P
V_P
V_{CC}
A_{OUT}
B_{OUT}
Connector
Circuitry
Under
Protection
V_N
Ground Rail

(Note 1)

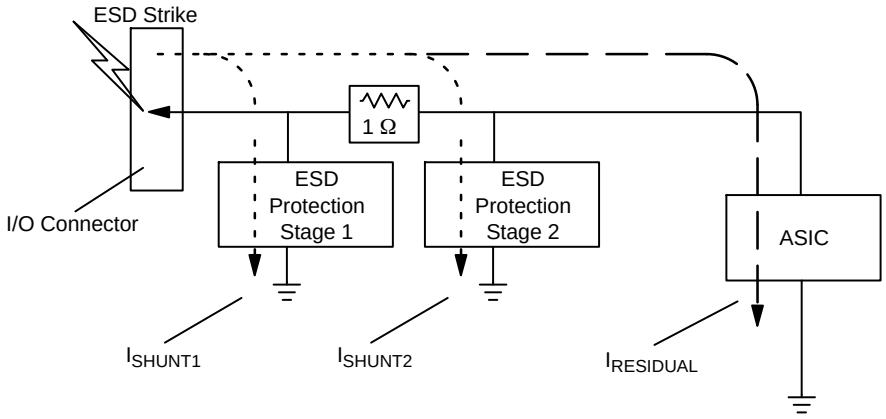
V_P	Operating Supply Voltage			5	5.5	V
I_{CC5}	Operating Supply Current	V_P = 5 V			1	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8 mA, T_A = 25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	V
V_{ESD}	ESD Protection, Contact Discharge per IEC 61000−4−2 Standard OUT−to−V_N Contact IN−to−V_N Contact	T_A = 25°C	 ±12 ±4			kV
I_{RES}	Residual ESD Peak Current on RDUP (Resistance of Device Under Protection)	IEC 61000−4−2 8 kV RDUP = 5 Ω, T_A = 25°C		2.3		A
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	I_{PP} = 1 A, T_A = 25°C, t_P = 8/20 μs, Zap at OUT, Measure at IN		 +9 –1.4		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1 A, T_A = 25°C, t_P = 8/20 μs, Zap at OUT, Measure at IN		 0.4 0.3		Ω
C_{OUT}	OUT Capacitance	f = 1 MHz, V_P = 5.0 V, V_{IN} = 2.5 V, V_{OSC} = 30 mV (Note 2)		1.5		pF
ΔC_{OUT}	Channel to Channel Capacitance Match	f = 1 MHz, V_P = 5.0 V, V_{IN} = 2.5 V, V_{OSC} = 30 mV		0.02		pF
R_S	Series Resistance			1		Ω
ΔR_S	Channel to Channel Resistance Match			±10	±30	mΩ

1. All parameters specified at T_A = –40°C to +85°C unless otherwise noted.
2. Capacitance measured from OUT to V_N with IN floating.

The following sections describe the standard single clamp ESD protection device and the dual clamp ESD protection architecture of the CM1231−02SO.

Conceptually, an ESD protection device performs the following actions upon a strike of ESD discharge into the protected ASIC (see Figure 1).

1. When an ESD potential is applied to the system under test (contact or air



The PicoGuard XP™ two−stage per channel matched clamp architecture with isolated clamp rails features a series element to radically reduce the residual ESD current (I_{RES}) that enters the ASIC under protection (see Figure 3). From stage 1 to stage 2, the signal lines go through matched dual 1 Ω resistors.

The function of the series element (dual 1 Ω resistors for the CM1231−02SO) is to optimize the operation of the stage two diodes to reduce the final I_{RES} current to a minimum while maintaining an acceptable insertion impedance that is negligible for the associated signaling levels.

Each stage consists of a traditional low−cap Dual Rail Clamp structure which steer the positive or negative ESD

Figure 4 illustrates a single stage ESD protection device. The inductor element represents the parasitic inductance arising from the bond wire and the PCB trace leading to the ESD protection diodes.

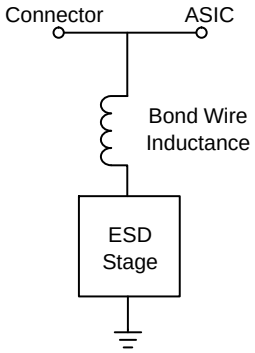
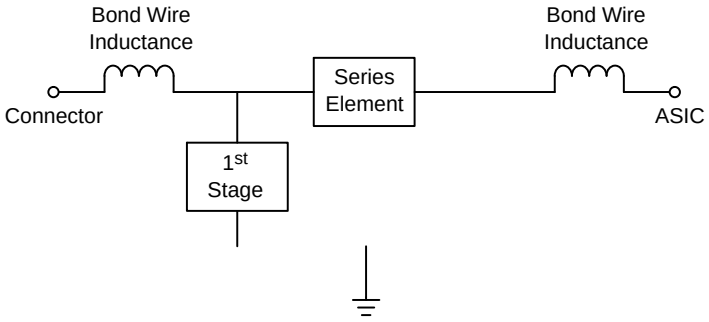
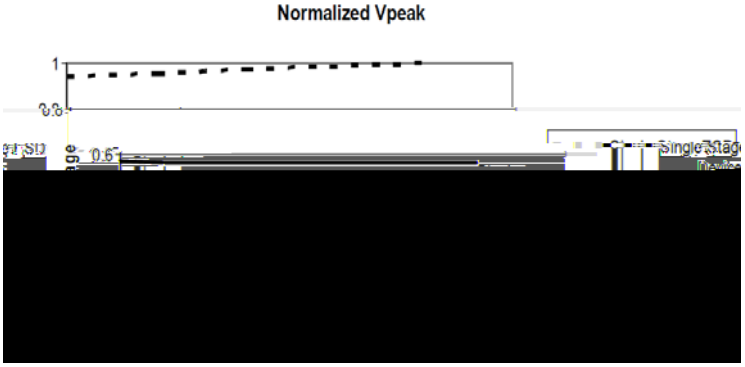
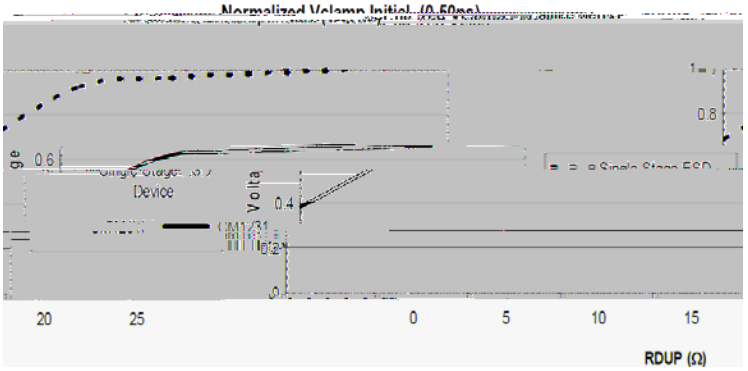


Figure 5 illustrates one of the two CM1231−02SO channels. Similarly, the inductor elements represent the parasitic inductance arising from the bond wire and PCB traces leading to the ESD protection diodes as well.

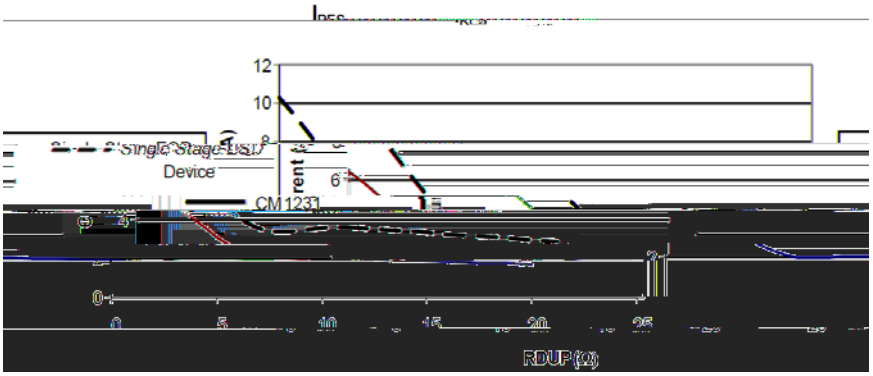


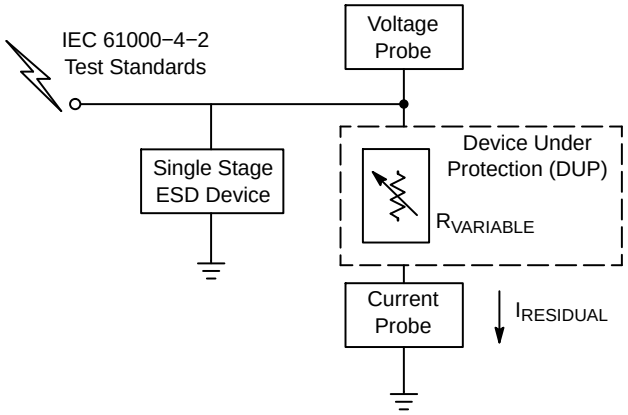
The following graphs (see Figure 6, Figure 7 and Figure 8) show that the CM1231−02SO (dual stage ESD protector) lowers the peak voltage and clamping voltage by 40% across a wide range of loading conditions in comparison to a standard single stage device. This data was derived using the test setups shown in Figure 9 and Figure 10.

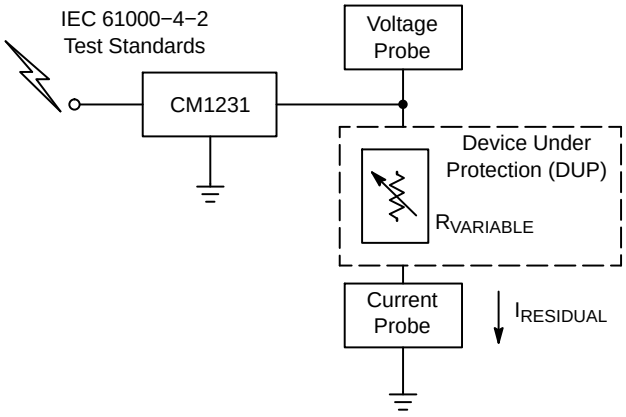


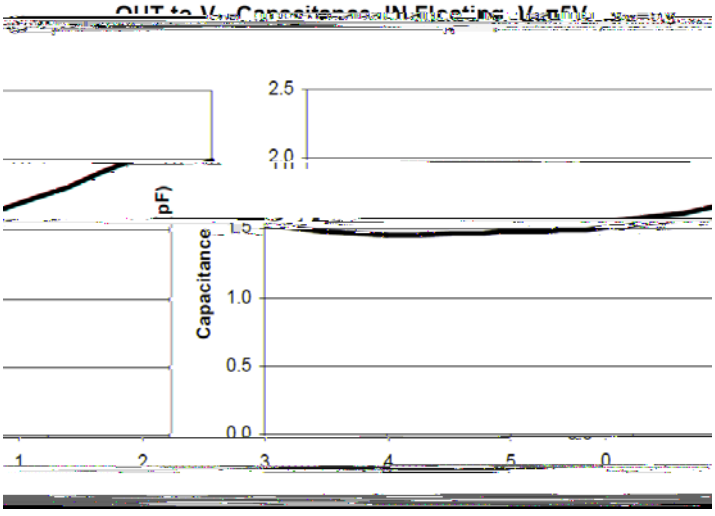


*RDUP indicates the amount of Resistance (load) supplied to the Device Under Protection (DUP) through a variable resistor.



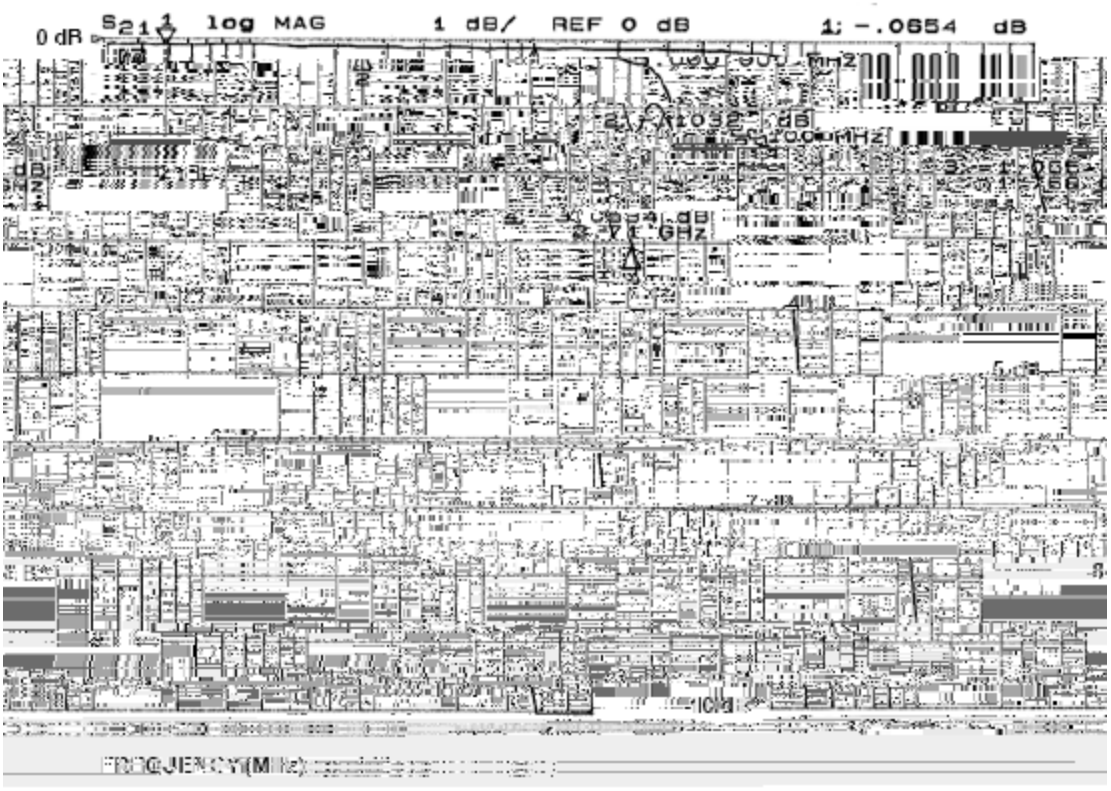

IEC 61000−4−2
Test Standards
Voltage
Probe
Single Stage
ESD Device
Device Under
Protection (DUP)
RVARIABLE
Current
Probe
IRESIDUAL


IEC 61000−4−2
Test Standards
Voltage
Probe
CM1231
Device Under
Protection (DUP)
RVARIABLE
Current
Probe
IRESIDUAL


2.5
2.0
pF)
Capacitance
1.0
0.5
0.0
1
2
3
4
5
0

–

Ω



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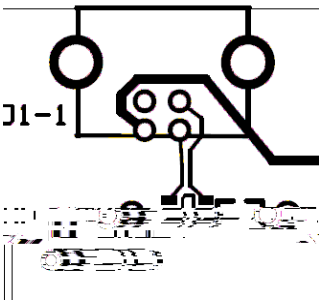
The CM1231−02SO has an integrated zener diode between V_P and V_N (for each of the two stages). This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the zener breakdown voltage, it is recommended that a 0.22 μF ceramic chip capacitor be connected between V_P and the ground plane.

With the CM1231−02SO, this additional bypass capacitor is generally not required.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

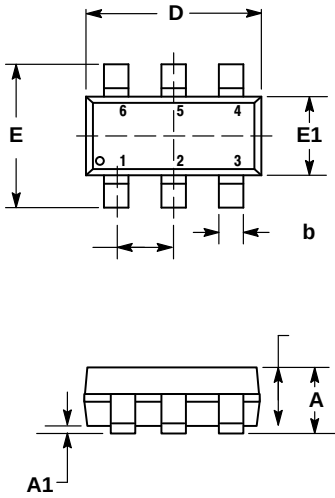


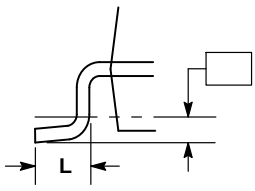
See also ON Semiconductor Application Note, “Design Considerations for ESD Protection,” in the Applications section.

SOT 23, 6 Lead
CASE 527AJ
ISSUE B

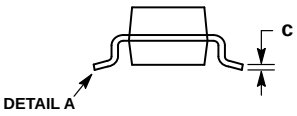
DATE 29 FEB 2012

SCALE 2:1





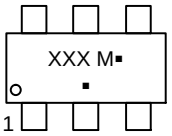
DETAIL A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.